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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,983	07/30/2003	Hideharu Koike	500-002	7730

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EXAMINER	
NGUYEN, HAI L	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 02/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,983	KOIKE, HIDEHARU	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *See Continuation Sheet*.

Continuation of Attachment(s) 6). Other: a copy of the definition of the inverter (2 pages).

DETAILED ACTION

Response to Amendment

1. The amendment received on 12/15/04 has been reviewed and considered with the following results:

As to the prior art rejections to claims 1-6, Applicant's arguments with respect to the prior art rejections by the previous office action mailed on 08/11/2004 have been fully considered but are not deemed to be persuasive. Therefore, the prior art rejection is maintained. The arguments supporting the previous rejections are addressed in detail below.

As to the prior art rejections to claims 7-14 made in the previous Office Action are now withdrawn in view of Applicant's amendments. However, Applicant's amendments necessitate new ground of rejection as set forth below.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 7-14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The new added limitation "said transition circuit comprising with a Pch MOS transistor and a Nch MOS transistor; the source of said Pch MOS transistor and the Nch MOS

transistor being coupled with the input of said transition circuit; the drain of said Pch MOS transistor and the Nch MOS transistor being coupled with the output of said transition circuit; the gate of said Pch MOS transistor being coupled with a first reference voltage; the gate of said Nch MOS transistor being coupled with a second reference voltage" in the claims is new matter since it is not recited in the originally filed application.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 13 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 13, the limitation "a reference voltage of said transition circuit" lacks clear antecedent basis. It is unclear if this reference voltage is referred to either "a first reference voltage" or "a second reference voltage" recited in claim 7 (or a different "reference voltage").

Claim 14 is rejected due to its dependencies on claim 13.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-3, 5, and 6 remain rejected, as per the previous office action, under 35 U.S.C. 103(a) as being unpatentable over Gans et al. (US 6,353;521; previously cited) in view of Konno (US 5,914,516; previously cited).

With regard to claim 1, Gans et al. discloses in Fig. 2 an integrated circuit comprising a CMOS inverter (5), the input of the CMOS inverter being coupled with an input pad (25) of the integrated circuit, the output of the CMOS inverter being coupled with an input buffer (51). Fig. 2 of Gans et al. shows a circuit meeting all of the claimed limitations, except for a first capacitor (212 in instant Fig.2) being inserted between the output of the CMOS inverter and a first voltage source; and a second capacitor (213) being inserted between the output of the CMOS inverter and a second voltage source, note that it also means the first and second capacitors being inserted between the input (N1) of the input buffer (14) and the first and second voltage sources, respectively. Konno teaches in Fig.3 a circuit having a first capacitor (14) being inserted between the input (3) of the input buffer (2) and a first voltage source (4) and a second capacitor (15) being inserted between the input of the input buffer and a second voltage source (7) as recited in the claim. Therefore, it would have been obvious to one of ordinary skill in the art to implement those capacitor taught by Konno with the prior art (Fig. 2 of Gans et al.) in order to improve the surge protection function.

With regard to claims 2 and 3, the above discussed circuit of the references meets all of the claimed limitations except for Gans et al. does not disclose that the integrated circuit is a LSI or a VLSI. However, it would have been obvious to one of ordinary skill in the art to realize that any integrated circuit (many types of which are well known in the art including a LSI or a VLSI as recited in the claims) can benefit from the circuit taught by the references for the advantage of

being able to improve the surge protection function of the integrated circuit. Therefore, the claimed invention does not define patentably over the circuitry of the references.

With regard to claims 5 and 6, the references also meet the recited limitations in these claims.

8. Claim 4 remains rejected, as per the previous office action, under 35 U.S.C. 103(a) as being unpatentable over Gans et al. in view of Konno, as applied to claim 1 above, and further in view of the admitted prior art, Fig. 1 in the present application.

With regard to claim 4, the above-discussed circuit of the references meets all of the claimed limitations except that the buffer circuit (51 in Fig. 2 of Gans et al.) is not a Schmitt-trigger type buffer circuit. The admitted prior art (Fig. 1 in the present application) shows a circuit having a Schmitt trigger (14) as a buffer circuit. Since the admitted prior art and the circuit of the references are similar, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made utilize a Schmitt trigger circuit as the buffer circuit (51 in Fig. 2 of Gans et al.) in the references' circuit in order to remove any noise spikes around the threshold point of its input on both the rising and falling edges of the input signal.

9. Claims 7-12 are rejected, under 35 U.S.C. 103(a) as being unpatentable over Kim (US 6,724,226) in view of Konno.

With regard to claims 7 and 10, Kim discloses in Fig. 2 an integrated circuit comprising a transition circuit (T2, T3), the input of the transition circuit being coupled with an input pad (11) of the integrated circuit, the output of the transition circuit being coupled with an input buffer (17), the transition circuit comprising with a Pch MOS transistor (T3) and a Nch MOS transistor (T2); the source of the Pch MOS transistor and the Nch MOS transistor being coupled with the

input of the transition circuit; the drain of the Pch MOS transistor and the Nch MOS transistor being coupled with the output of the transition circuit; the gate of the Pch MOS transistor being coupled with a first reference voltage (D); the gate of the Nch MOS transistor being coupled with a second reference voltage (Vdd1). Fig. 2 of Kim shows an integrated circuit meeting all of the claimed limitations, except for a first capacitor being inserted between the output of the transition circuit and a first voltage source; and a second capacitor being inserted between the output of the transition circuit and a second voltage source. Konno teaches in Fig. 3 a similar integrated circuit having a first capacitor (14) being inserted between the output of the transition circuit (by given the broadest reasonable interpretation; elements 11, 12, 13 is the transition circuit because it has a function of transferring signal from input to the output) and a first voltage source (4); and a second capacitor (15) being inserted between the output of the transition circuit and a second voltage source (7) as recited in the claim. Therefore, it would have been obvious to one of ordinary skill in the art to implement those capacitor taught by Konno with the prior art (Fig. 2 of Kim) in order to improve the surge protection function.

With regard to claims 8 and 9, the above discussed circuit of the references meets all of the claimed limitations except for Konno does not disclose that the integrated circuit is a LSI or a VLSI. However, it would have been obvious to one of ordinary skill in the art to realize that any integrated circuit (many types of which are well known in the art including a LSI or a VLSI as recited in the claims) can benefit from the circuit taught by the references for the advantage of being able to improve the surge protection function of the integrated circuit. Therefore, the claimed invention does not define patentably over the circuitry of the references.

With regard to claim 11, the input buffer circuit (17 in Fig. 2 of Kim) is a Schmitt-trigger.

With regard to claim 12, the first voltage source is VDD (Vdd1).

Response to Arguments

10. Applicant's first argument concerning that "the Gans patent fails to disclose or suggest the claimed CMOS inverter as an input buffer", page 6 lines 14-15, is not persuasive because no such limitation is recited in the claims.

11. Applicant's second argument concerning that "the circuit 5 does not work as inverter", page 7 line 2, is not persuasive because it is well-known in the electronics art that the inverter is a circuit with one input and one output, and its function is to invert the input (see attached copy of the definition of the inverter). When the input is high, the output is low, and vice versa. The circuit 5 (in Fig. 2) of Gans et al. clearly has that function. For example, when the input level increases to a certain high level, transistor 20 is on, and causes node 30 (output of circuit 5) low; and when the input level decreases to a certain low level, transistor 15 is on, and causes node 30 high. Therefore, the circuit 5 of the reference meets the recited limitation as inverter in claim 1. Thus, the rejections of record are still believed to be proper and are therefore maintained

Conclusion

12. Regarding claims 13 and 14, the patentability thereof cannot be determined because of their indefiniteness.

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN
February 1, 2005

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